Analysing Manycore OS Design Aspects in NIX

Gorka Guardiola
paurea@lsub.org
LSUB
Rey Juan Carlos Univ.

Noah Evans
Jim McKie
Bell Labs

Ron Minnich
Google

Charles Forsyth
Vita Nuova

Fco. J. Ballesteros
Enrique Soriano
Rey Juan Carlos Univ.
What is NIX?

- Joint work, Bell Labs, Rey Juan Carlos Univ., Vitanuova, Sandia Nat. Labs
- Based on Plan 9
- Rethink OS abstractions and assumptions for new multicore machines
- Try to keep the kernel in charge of policies
Roles

Kernel space/user space **core** specialization

- Only kernel
- Timesharing
- Only user

Traditional scheme

NIX scheme
Roles

Kernel space is in a core with kernel
Roles

- Mechanisms: **may not have coherent memory** (the implementation does for now)
- Processors may be specialized (hw)
- Assign roles **automatically**, wip
- New roles (XC), wip
- Automatic assignment, policies, wip
Scheduler
Scheduler
Scheduler

- Found that adding cores made compiling a kernel slower (K10 magny cours, 32 cores)
- AMP vs SMP
- NUMA aware
- Latency aware? (not in ACPI info)
- Probably the next bottleneck is in spinlocks, find which, segregate the resources when possible, wip
No questions :-)
I have some questions myself

- I have some, latency vs. bandwidth vs. CPU bound
- ACPI information on latency
- How do different architectures compare